Trapping Effects in Wide-Bandgap Microwave FETs

S. C. Binari, P. B. Klein, and T. E. Kazior†

Naval Research Laboratory, Washington D.C. 20375
†Raytheon RF Components, Andover MA 07870

Abstract — **It is well known that trapping effects can limit the output power performance of microwave field-effect transistors. This is particularly true for the wide-bandgap devices. In this paper, we review the various trapping phenomena observed in SiC and GaN-based FETs that contribute to compromised power performance. For both of these material systems, trapping effects associated with both the surface and with the layers underlying the active channel have been identified.**

I. INTRODUCTION

In recent years, both SiC and GaN-based FETs have demonstrated impressive microwave performance, with SiC MESFETs producing 4.6 W/mm at 3.5 GHz [1] and AlGaN/GaN HEMTs exhibiting 9.8 W/mm at 8 GHz [2]. Although these results have set the state-of-the-art for microwave power density, it is generally recognized that significant developmental work remains for these technologies to become viable. An area of particular concern is the limiting effect of electronic traps on microwave power performance [3-7]. Traps influence power performance through the formation of quasi-static charge distributions, most notably on the wafer surface or in the buffer layers underlying the active channel. This parasitic charge acts to restrict the drain current and voltage excursions, thereby limiting the high-frequency power output.

In this paper, the current issues associated with trapping in AlGaN/GaN HEMTs and GaN MESFETs, and to a lesser extent SiC MESFETs, will be reviewed. A variety of trapping effects have been observed, including transconductance frequency dispersion, current collapse of the dc drain characteristics, gate- and drain-lag transients, and restricted microwave power output. Significant research activity has been directed toward understanding and eliminating these effects [8]. Similar trapping problems were faced during the development of the GaAs technology (see summary in ref. 8), and it is apparent that much of the knowledge obtained and techniques utilized for the GaAs case can be applied to the present situation in the wide-bandgap devices.

II. TRAPPING EFFECTS IN GaN-BASED FETs

In principle, trapping centers can reside at the surface, in the AlGaN barrier layer, at the 2-DEG interface, or in the GaN buffer layer. While it is known that defects exist in the AlGaN layer, a correlation with compromised microwave performance has not been established. This holds true for states at the AlGaN/GaN interface as well, although their presence is expected to limit the 2-DEG channel mobility. Although there are a variety of conflicting explanations for the observed trapping effects, the picture that seems to be emerging is that trapping at the surface and in the underlying buffer layers are primarily responsible for compromised microwave power performance. Consequently, the discussion that follows will be divided between trapping phenomena associated with these two regions.

It should also be noted that the nitrides are characterized by a high concentration (typically 10^8 to 10^{10} cm^{-2}) of dislocations. A number of studies have shown that electrically-active trapping centers can exist in the vicinity of these extended defects. However, there is little information to directly link specific traps and trap-related phenomena with dislocations. Consequently, while some of the trapping phenomena discussed below may eventually be shown to result from defects localized at dislocations, we are currently unable to distinguish these from traps located elsewhere in the material.

A. Buffer trapping: current collapse

Current collapse refers to the persistent (yet recoverable) reduction of the dc drain current that results from the application of a high drain-source bias. Current collapse in a nitride-based FET was first reported in an AlGaN/GaN HEMT by Khan et al. [8]. It has also been observed in GaN MESFETs [9], where current collapse was interpreted in terms of deep traps in the high-resistivity (HR) OMVPE GaN buffer layer, which is grown under conditions that enhance trap formation in order to compensate the shallow donors and produce HR material. Further studies [5] confirmed the location of the traps in the HR GaN buffer layer, as collapse was not observed in devices grown on conducting substrates: the traps in the structure were already filled by compensating shallow donors.

By studying the wavelength dependence of the drain current recovery of GaN MESFETs in detail, Klein et al. [10] were able to develop a method to provide spectroscopic signatures of the traps responsible for current collapse, and to estimate the trap depth relative to the band edges. These defects are located approximately 1.8 eV and 2.85 eV below the conduction band, respectively. It is interesting that each of these absorptions was also found to match published spectra of persistent photoconductivity (PPC) centers in GaN, indicating that these traps can induce both PPC and current collapse. Several other investigators (Zhang et al., Kuliev et al., Meneghesso et al., see ref. 9) have also assigned current collapse effects observed in GaN FETs to traps in the buffer layer.

Photoionization measurements have also been carried out in AlGaN/GaN HEMT structures [11]. The photoionization spectra were found to be similar to those of the GaN MESFET, exhibiting the two broad, trap-related absorptions and a rapid increase at the GaN bandgap. This work indicated that the same traps in the HR GaN buffer layer, that were responsible for current collapse in the MESFET, produced collapse in the HEMT as well. The current evidence would suggest that current collapse in nitride-based FETs grown by OMVPE is associated with traps in the HR GaN buffer layer related to carbon incorporation and to structural defects.

Recovery from current collapse by thermal emission of the trapped carriers has a characteristic time dependence, and the temporal response of the current collapse (i.e reduced drain current) can be investigated with drain lag measurements. A typical long-term drain lag characteristic has a recovery time on the order of minutes. It should be noted that devices fabricated on higher quality buffer layers are nearly free from current collapse and the associated drain lag.

B. Surface trapping in GaN FETs

It is widely acknowledged that surface states or surface charge can have a pronounced effect on the microwave performance of HEMTs. As in the GaAs case, surface trapping can generally be identified through gate lag measurements. A number of groups have used this approach to study the effect of trapping on GaN devices. The association between gate lag and surface trapping is generally established by correlating gate lag with changes made to the device surface through techniques such as chemical treatment or dielectric passivation. Binari et al. [8] associated gate lag with the presence of surface trapping in the device access regions. Similar to GaAs FETs, they observed a direct correlation between gate lag and output power in unpassivated GaN HEMTs. By adding a silicon nitride passivation layer, a dramatic improvement in drain current response was observed.

Trassaert et al. [12] observed a significant difference between the dc and pulsed I-V characteristics of unpassivated GaN MESFETs. They concluded that the traps responsible for the difference between the dc and pulsed characteristics are associated with surface states. Others have utilized pulsed I-V measurements, to provide information on trapping effects and have correlated these measurements with microwave power performance [13, 14]. Kazior et al [13] found that unpassivated devices tended to exhibit significantly compressed pulsed I-V characteristics and this was correlated with poor microwave power performance. Passivation was found to reduce the pulsed I-V compression with a concomitant improvement in RF power. Passivation presumably establishes a near-optimal dielectric/semiconductor interface that best neutralizes the net surface charge arising from the combination of a polarized AlGaN barrier and surface states associated with surface defects, dangling bonds and adsorbed ions or charged residuals. Several other groups [see ref 8] have reported on the effect of silicon nitride passivation on microwave power performance. Due to the reduction of surface trapping, increases in output power from 20% to a factor of 2 have been observed relative to the unpassivated case. However, devices passivated with nominally the same passivation process and surface pretreatment exhibit varying degrees of pulsed I-V current compression, suggesting that the reduction in pulsed I-V current compression is a strong function of surface and material quality.

While the pulsed measurements referred to above can be thought of as approximating large-signal conditions, it is possible to directly measure the drain current under large-signal gate voltage drive. This has been done as a function of frequency [15-17], and transition frequencies varying over a very large range (10^{-3} Hz to 10 GHz) were observed. Large reductions in the current amplitude were observed over this frequency range, which translates directly into lower power outputs. This dispersion was attributed to piezo-related charge states at the surface, which create a parasitic gate between the gate and drain. This parasitic gating concept is analogous to that described for GaAs devices. In related large-signal measurements, Nguyen et al. [4] observed changes in the dc drain current of GaN HEMTs as a function of the input RF drive. To identify the location of the responsible traps they performed RF measurements as a function of gate bias. It was concluded that the drain current compression under RF drive is due to traps located either in the AlGaN barrier or at the surface, and not due to trapping of hot electrons in the buffer layer (i.e. current collapse).

III. TRAPPING EFFECTS IN SiC MESFETs

Similar to GaN, SiC exhibits a high breakdown field and a high saturated electron velocity. Silicon carbide also offers a high thermal conductivity, making it a natural choice for high-power electronics. Although nitride-based HEMT structures can attain considerably higher frequency response, the frequency-power-bandwidth design tradeoffs between SiC MESFETs and GaN HEMTs are not well established, and the SiC MESFET may offer advantages for total power output due to its lower input capacitance [18]. The SiC technology is certainly more mature than that of GaN. However, SiC MESFETs are not without trapping problems associated with both the surface and with the layers underlying the active channel.

It was observed by Noblanc et *al.* [19, 20] that the drain current of devices fabricated on semi-insulating (SI) SiC substrates decayed with time, with a time constant on the order of seconds. The current could be restored by removing the drain bias for several seconds. As a result of this effect, the RF power output of these devices was observed to be inferior to that of devices grown on n^+ substrates. The drain current decay was also found to be much less severe for devices grown on n^+ substrates than on SI substrates. In addition, with increasing negative gate bias, the effect became more severe. It was thus concluded that the traps responsible for this effect were probably associated with the SI substrate or the substrate/p-buffer layer interface. Further work by these authors [21] probed the sensitivity of this trapping effect to variations in the thickness and doping level of the p-type buffer. While the dc drift could be almost eliminated by using a thicker buffer, a rapid (μsec) decay of the drain current persisted if an RF signal was applied to the gate, leading to a reduction in the RF output power. It was concluded that the trapping effect was caused by the injection of carriers from the channel into the p-buffer, similar to the mechanism of current collapse discussed above, and that the effect was dependent upon the depletion state of the buffer layer. In fact, the dc I-V characteristics before and after high voltage biasing clearly indicated a collapse of the drain current.

In addition to the substrate/buffer layer trapping discussed above, drain current transients related to surface trapping have also been observed in SiC MESFETs [22, 23]. It was observed [22] that if the gate recess etch damage was removed from the ungated surface regions between the gate and the source and drain, the drain current decay was decreased substantially. After passivating the channel recess and placing the gate in a second channel recess cut through the passivation [23], the dc drain current transient was essentially eliminated.

Siriex et al. [24] advanced work on substrate trapping by carrying out pulsed I-V and S-parameter measurements (with varying gate and drain quiescent levels) on MESFETs grown on SI substrates. Measurements were carried out on several devices grown with varying buffer layer thickness and doping. It was reported [6] that channel carrier injection was successfully reduced or eliminated by this procedure. Additionally, the conductance dispersion was studied as a function of temperature in order to extract trap parameters. It was concluded that a trap with activation energy of 1.07 eV was involved, which was tentatively identified as due to vanadium defects.

IV. CONCLUSION

Although outstanding microwave power performance has been demonstrated with both SiC and GaN-based FETs, significant issues remain regarding the further development of these technologies. One prominent issue is the limiting effect of electronic traps on the device microwave power performance. Similar trapping problems were faced during the development of the GaAs technology, and it is apparent that much of the knowledge obtained and techniques utilized for the GaAs case can be applied to the present situation in the wide bandgap devices.

Although the SiC technology is more mature than that of GaN, SiC MESFETs still suffer from trapping-related issues. Trapping associated with the SiC substrate is apparent, but buffer layer solutions to the substrate trapping problem have yielded promising results. Surface-related trapping has been shown to affect device performance, and passivation and gate-recess schemes have been utilized to minimize this effect.

Considerably more work has been published on trapping in GaN FETs than on SiC devices. While it is clear that trapping effects play a significant role in the performance observed in GaN-based FETs, the relative immaturity of the GaN-based material system and the variations between laboratories in device design, material quality, and device processing complicate the understanding of trapping in these devices. At this point in time there is considerable evidence to show that current collapse of the dc device characteristics is related to the presence of traps in the GaN buffer layer. Surface trapping has been shown to be minimized through the use of dielectric passivation, though with variable degrees of success. Both sources of trapping result in compromised microwave power performance. We anticipate that device performance will be improved and trapping phenomena will continue to be minimized through further improvements in the materials growth and process technology for these two materials systems.

ACKNOWLEDGMENT

This work was supported by the Office of Naval Research. The authors which to thank their colleagues at the Naval Research Laboratory and at Raytheon for many fruitful discussions on this topic.

REFERENCES

[1] S. T. Allen, W. L. Pribble, R. A. Sadler, T. S. Alcorn, Z. Ring, and J. W. Palmour, "Progress in high power SiC Microwave MESFETs," in IEEE MTT-S Digest, pp. 321-324, 1999.

[2] Y. -F. Wu, D. Kapolnek, J. Ibbetson, N.-Q. Zhang, P. Parikh, B. P. Keller, and U. K. Mishra, "High Al-content AlGaN/GaN HEMT on SiC substrates with very-high power performance," in International Electron Device Meeting Digest, pp. 925-927, 1999.

[3] J. C. Zolper, "Progress towards ultra-wideband AlGaN/GaN MMICs," Solid-State Electronics, vol. 43, pp. 1479-1482, 1999.

[4] C. Nguyen, N. X. Nguyen, and D. E. Grider, "Drain current compression in GaN MODFETs under large-signal modulation at microwave frequencies," Electronics Lett., vol. 35, pp. 1380-1382, 1999.

[5] S. C. Binari, K. Ikossi, J. A. Roussos, W. Kruppa, D. Park, H. B. Dietrich, D. D. Koleske, A. E. Wickenden, and R. L. Henry, "Trapping Effects and Microwave Power Performance in AlGaN/GaN HEMTs," IEEE Trans. ED, vol. 48, pp. 465-471, 2001.

[6] N. Sghaier, A. K. Souifi, J-. M. Bluet, M. Berenguer, G. Guillot, O. Noblanc, and C. Brylinski, "Influence of interface states on output conductance on 4H-SiC MESFETs on semi-insulating substrate," Mat. Res. Soc. Symp., Vol. 640, pp. H4.4.-H4.4.6, 2001.

[7] E. Morvan, O. Noblanc, C. Dua, and C. Brylinski, "SiC Microwave Power Devices," Materials Science Forum Vols., 353-356, pp. 669-674, (2001).

[8] S. C. Binari, P. B. Klein, and T. E. Kazior, "Trapping Effects in GaN and SiC Microwave FETs," IEEE Proceedings, 2002, in press, and references therein.

[9] S. C. Binari, W. Kruppa, H. B. Dietrich, G. Kelner, A. E. Wickenden, and J. A. Freitas, Jr., "Fabrication and characterization of GaN FETs," Solid-State Electronics, vol. 41, pp. 1549-1554, 1997.

[10] P.B. Klein, J.A. Freitas, Jr., S.C. Binari and A.E. Wickenden, "Observation of deep traps responsible for current collapse in GaN metal semiconductor field effect transistors", *Appl. Phys. Lett.*, vol. 75, pp. 4016-4018, 1999.

[11] P. B. Klein, S. C. Binari, K. Ikossi-Anastasiou, A. E. Wickenden, D. D. Koleske, R. L. Henry and D. S. Katzer, "Investigation of traps producing current collapse in AlGaN/GaN high electron mobility transistors", Electron. Lett., vol. 37, pp. 661-662, 2001.

[12] S. Trassaert, B. Boudart, C. Gaquière. D. Théron, Y. Crosnier, F. Huet, and M. A. Poisson, "Trap effects studies in GaN MESFETs by pulsed measurements," Electron. Lett., vol. 34, pp. 1386-1388, 1999.

[13] T. E. Kazior et al, presented at Second Workshop GaN Electronics, 2001.

[14] Y-.F. Wu, B. P. Keller, S. Keller, J. J. Xu, B. J. Thibeault, S. P. Denbassrs, and U. K. Mishra, "GaN-based FETs for microwave power amplification," IEICE Trans. Electron., Vol. E82-C, pp. 1895-1905, 1999.

[15] E. Kohn, I. Daumiller, P. Schmid, N. X. Nguyen, and C. N. Nguyen, "Large signal frequency dispersion of AlGaN/GaN heterostructure field effect transistors," Electronics Lett., Vol. 35, pp. 1022-1023, 1999.

[16] I. Daumiller, D. Theron, C. Gaquiere, A. Vescan, R. Dietrich, A. wieszt, H. Leier, R. Vetury, U. K. Mishra, I. P. Smorchkova, S. Keller, N. X. Nguyen, C. Nguyen, and E. Kohn, "Current instabilities in GaN-based devices," IEEE Electron Device Lett., Vol. 22, pp. 62-64.

[17] R Vetury, N. Q. Zhang, S. Keller, U. K. Mishra, " The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," IEEE Trans. Electron Devices, Vol. 48, pp. 560 -566, 2001.

[18] J. W. Palmour. S. T. Allen, S. T. Sheppard, W. L. Pribble, R. A. Sadler, T. S. Alcorn, Z. Ring, and C. H. Carter, Jr., "Progress in SiC and GaN microwave devices fabricated on semi-insulating 4H-SiC substrates," in Device Research Conf. Digest, pp. 38-41, 1999.

[19] O. Noblanc, C. Arnodo, E. Chartier and C. Brylinski, "Characterization of power MESFETs on 4H-SiC conductive and semi-insulating wafers," Materials Science Forum, vol. 264-268, p. 949-952, 1998.

[20] O. Noblanc, C. Arnodo, C. Dua, E. Chartier and C. Brylinski, "Power density comparison between microwave power MESFETs processed on conductive and semi-insulating wafer," Material Science Forum, vol. 338-342, p. 1247-1250, 2000.

[21] O. Noblanc, C. Arnodo, C. Dua, E. Chartier and C. Brylinski, "Progress in the use of 4H-SiC semi-insulating wafers for microwave power MESFETs," Mater. Science and Eng. B, vol. 61-62, p. 339-344, 1999.

[22] K. P. Hilton, M. J. Uren, D. G. Hayes, P. J. Wilding, H. K. Johnson, J. J. Guest, and B. H. Smith, "Surface induced instabilities in 4H-SiC microwave MESFETs," Materials Science Forum Vols. 338-342, pp. 1251-1254, 2000.

[23] K.P. Hilton, M.J. Uren, D.G. Hayes, P.J. Wilding, and B.H. Smith, "Suppression of instabilities in 4H-SiC microwave MESFETs," in *High Performance Electron Devices for Microwave and Optoelectronic Applications, 2000," (IEEE, 2000)*, p. 67-70.

[24] D. Siriex, D. Barataud, R. Sommet, O. Noblanc, Z. Ouarch and C. Brylinski, "Characterization and modeling of nonlinear trapping effects in power SiC MESFETs," in 2000 IEEE MTT-S Digest, vol. 2, p. 765-768, 2000.